DATA HOLDING DISPLAY APPARATUS, DRIVING METHOD THEREOF, AND TELEVISION SET

This nonprovisional application claims priority under 35 U.S.C. § 119(a) on Patent Application No.2003-100725 filed in Japan on April 3, 2003, the entire contents of which are hereby incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to a display apparatus using display devices that can hold data, and particularly relates to a technique for improving moving image performance of a display apparatus having group of display devices that are arranged in a matrix manner.

BACKGROUND OF THE INVENTION

In a conventional display apparatus such as a TV set,

CRT (Cathode Ray Tube) has prevailed. Recently, however, the performances such as viewing angle, contrast, color reproducibility has been improved apart from space saving and power saving features. A liquid crystal display apparatus of matrix type is successor to the CRTs.

The liquid crystal display apparatus of matrix type has a display area provided with a plurality of scanning signal lines, a plurality of data signal lines that are provided so as to be perpendicular to and to intersect with the scanning signal lines, TFTs (Thin Film Transistors) as control switches each provided at each intersection of the scanning signal lines and the data signal lines. The liquid crystal display apparatus is further provided with (a) a scanning signal line driving circuit (gate driver) for outputting the scanning signals to the scanning signal lines, (b) a data signal line driving circuit (data driver) for outputting to the data signal lines the display signals corresponding to display data, and (c) a control circuit (controller) for controlling the scanning signal line driving circuit and the data signal line driving circuit, respectively. With the arrangement, the display signal is applied to a pixel electrode connected to the TFT that has been selected in response to the scanning signal, so as to control the alignment of the liquid crystal pixels in response to the difference of voltages between the pixel electrode and the opposed electrode.

The liquid crystal is capacitive load. On this account, when a display signal voltage is applied to the pixel electrode, the liquid crystal has the holding property in which the alignment, varying depending on the display signal voltage thus applied, is held. Because of this property, unlike the CRT, it is possible to obtain a display screen without flickering, unlike the CRT. On the other hand, the response speed of the liquid crystal itself, especially the response to halftone is not enough in one frame period of image input signal, thereby arising the problem that the residual image is found in the moving image.

Further, in the liquid crystal display apparatus, the display signal, which has been written into a corresponding pixel, keeps to be held during a time period in which the TFT is not selected. On this account, even if the response speed of the liquid crystal is made fast, the residual image exists on the retina. This is because human being follows one's eyes to the moving image. Thus, another problem arises that the display quality deteriorates.

In view of the circumstances, the following liquid crystal method is proposed in the Japanese unexamined patent publication No. 11-109921 (publication date: April 23, 1999) which corresponds to U.S. Patent (USP 6,396,469 B1), so as to solve the foregoing problems.

According to the arrangement disclosed in the publication, a screen is divided into upper and lower screens (a) such that the signal scanning for the upper screen and a black signal (blanking) scanning for the lower screen are simultaneously carried out during the first half of one frame period, and (b) such that the signal scanning for the lower screen and a black signal (blanking) scanning for the upper screen are simultaneously carried out during the second half of the one frame period.

With the arrangement, when focusing attention on a specific pixel, it is inevitable that both image display period and black display period exist in one frame period. Especially, the existence of the black display period ensures that the image can be displayed without mixing the prior and subsequent frame data. It is possible to improve the display performance of moving image, accordingly.

The conventional arrangement, however, results in that the black display is always carried out on either one of the upper and lower screens in one frame period, thereby causing that the entire brightness of the display screen is lowered.

SUMMARY OF THE INVENTION

The present invention is made for solving the

foregoing problems, and its object is to provide a data holding display apparatus, a driving method thereof, and a television set each of which can avoid that the display quality is lowered due to the residual image found in the case of moving image display.

In order to achieve the object, a data holding display apparatus of the present invention includes (a) a display panel of data holding type, which is divided into a plurality of display sections each is capable of being independently driven, and in which a display signal is written into data signal lines connected to pixels of the display section that have been selected; (b) a plurality of data signal line driving circuits, provided for the respective display sections, for supplying the data signal line with the display signal corresponding to inputted display data; and (c) a control circuit for supplying each of the data signal line driving circuits with either one of the display data corresponding to input image signal and interpolation display data prepared in accordance with the input image signal during at least one time period among a plurality of time periods in one cycle in a displaying of the display panel, whereas supplying the each of the data signal line driving circuits with the other one of the display data and the interpolation display data during at least one other time period among the plurality of time periods.

With the arrangement, the data signal line driving circuits in the respective display sections are supplied with either one of the display data corresponding to an input image signal and interpolation display data prepared in accordance with the input image signal during at least one time period among a plurality of time periods in one cycle in a displaying of the display panel, whereas supplied with the other one of the display data and the interpolation display data during at least one other time period among the plurality of time periods. This gives rise to the result that the interpolation display data is written into the display section(s) other than the display section(s) into which the display data corresponding to the input image signal is written.

The reset of display can be made with respect to display section(s) because the interpolation display data is written into such display section(s) other than the display section(s) into which the display data corresponding to the input image signal is written. This makes it possible to restrain that the display quality of moving image is deteriorated due to the fact that a same display data has been held by a same pixel for a long period of time.

Further, it is possible to avoid that the brightness on a display screen is lowered, which occurs when the interpolation display data is merely set to a black display data. This is because the interpolation display data is

prepared in accordance with the input image signal.

Another data holding display apparatus in accordance with the present invention includes: (a) a display panel of data holding type for displaying a display signal, the display panel including: a plurality of scanning signal lines; a plurality of data signal lines provided so as to intersect with the scanning signal lines; and pixels provided in a matrix manner at respective intersections of the scanning signal lines and the data signal lines, the display panel having a display area which is divided, in a direction where the scanning signal lines are provided, into a plurality of display sections each capable of being independently driven, and in the display panel the display signal being written into data signal lines connected to pixels of the display section that have been selected, (b) scanning signal line driving circuit for sequentially selecting the scanning signal lines; (c) data signal line driving circuits, provided for the respective display sections, for supplying the data signal lines with the display signal corresponding to inputted display data; and (d) a control circuit for (1) controlling the scanning signal line driving circuit such that the scanning signal lines in the respective display sections are scanned collaterally and the scanning signal lines in the respective display sections are sequentially selected during a plurality of time periods of one cycle in a displaying of the display

panel, so as to repeatedly scan the respective display sections in the one cycle as many times as the number of the time periods, and (2) supplying the data signal line driving circuits of the respective display sections with either one of the display data corresponding to an input image signal and an interpolation display data prepared in accordance with the input image signal during at least one of the time periods whereas with the other during at least one other time period.

With the arrangement, it is possible to separately drive the display sections, which are obtained by dividing the display area of the display panel, collaterally by the respective data signal line driving circuits that correspond to the display sections. The scanning signal lines of the respective display sections are sequentially selected during the plural time periods (for example, the number of the time periods is equal to the number of display sections) in one cycle (for example, one frame). This ensures that the respective display sections are repeatedly scanned in the one cycle as many times as the number of the plural time periods. For example, the input image signal is decomposed to so as to correspond to the respective display sections, and the data signal line driving circuits of the respective display sections are supplied with either one of the display data corresponding to an input image signal and an interpolation display data

prepared in accordance with the input image signal during at least one of the time periods, whereas supplied with the other during at least one other time period.

Accordingly, it is not necessary in the present data holding display apparatus to scan the scanning signal lines of the respective display sections at a high speed. Because of this, it is possible to secure enough time for writing the display data into the pixel and to secure enough response time of the display panel to the writing.

On the other hand, from the viewpoint of the entire display panel, the double speed driving, i.e., the pseudo-double speed driving is carried out. This makes it possible to restrain that the display quality of moving image is deteriorated due to the fact that a same display data has been held by a same pixel for a long period of time.

Further, the interpolation display data is prepared in accordance with the input image signal. Accordingly, it is possible to avoid that the brightness on a display screen is lowered, which occurs when the interpolation display data is merely set to a black display data.

A further data holding display apparatus in accordance with the present invention includes: (a) a display panel of data holding type for displaying a display signal, the display panel including: a plurality of scanning signal lines; a plurality of data signal lines provided so as

to intersect with the scanning signal lines; and pixels provided in a matrix manner at respective intersections of the scanning signal lines and the data signal lines, the display panel having a display area which is divided, in a direction where the scanning signal lines are provided, into a plurality of display sections each capable of being independently driven, and in the display panel the display signal being written into data signal lines connected to pixels of the display section that have been selected, (b) scanning signal line driving circuit for sequentially selecting the scanning signal lines, and (c) data signal line driving circuits, provided for the respective display sections, for supplying the data signal lines with the display signal corresponding to inputted display data, the display area being divided into first and second display sections, the data holding display apparatus further including: (d) a control circuit for (1) controlling the scanning signal line driving circuit such that the scanning signal lines in the first and second display sections are sequentially scanned, respectively, during a first time period and a second time period that is adjacent to the first time period of one cycle in a displaying of the display panel, so as to repeatedly scan the respective first and second display sections twice in the one cycle, and (2) supplying the data signal line driving circuit of the first display section with the display data corresponding to an

input image signal during the first time period whereas with an interpolation display data prepared in accordance with the input image signal during the second time period, the control circuit supplying the data signal line driving circuit of the second display section with an interpolation display data prepared in accordance with the input image signal during the first time period whereas with the display data corresponding to the input image signal during the second time period.

With the arrangement, during the first time period of one cycle in a displaying of the display panel, the first display section displays an image corresponding to the input image signal and the second display section displays an interpolation image prepared in accordance with the input image signal, whereas, during the second time period, the first display section displays an interpolation image prepared in accordance with the input image signal and the second display section displays an image corresponding to the input image signal.

Accordingly, it is also not necessary in the present data holding display apparatus to scan the scanning signal lines of the respective display sections at a high speed. Because of this, it is possible to secure enough time for writing the display data into the pixel and to secure enough response time of the display means to the writing.

On the other hand, from the viewpoint of the entire display panel, the double speed driving, i.e., the pseudo-double speed driving is carried out. This makes it possible to restrain that the display quality of moving image is deteriorated due to the fact that a same display data has been held by a same pixel for a long period of time.

Further, the interpolation display data is prepared in accordance with the input image signal. Accordingly, it is possible to avoid that the brightness on a display screen is lowered, which occurs when the interpolation display data is merely set to a black display data.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a liquid crystal display apparatus in accordance with one embodiment of the present invention.

Fig. 2 is a circuit diagram showing an arrangement of a display section shown in Fig.1.

Fig. 3 is an explanatory diagram showing an input image signal supplied to a control circuit shown in Fig. 1 and showing input signals supplied to first and second

display sections, respectively.

Fig. 4 is an explanatory diagram showing how the respective input signals, supplied to the first and second display sections, are related.

Fig. 5 is a block diagram showing a display data generating section of the control circuit shown in Fig. 1.

Fig. 6 is an explanatory diagram showing interpolation display data that is generated by the display data generating section shown in Fig. 5.

Fig. 7 is a block diagram showing an arrangement in which an arithmetic circuit shown in Fig. 5 outputs an average of a current input image signal (the interpolation display data) and an input image signal corresponding to a previous frame, the current frame coming after such a previous frame.

Fig. 8 is a block diagram showing an arrangement in which the arithmetic circuit shown in Fig. 5 outputs the weighted interpolation display data.

Fig. 9 is a view showing a lookup table used as another arrangement in which the interpolation display data is generated by the display data generating section shown in Fig. 4.

Fig. 10 is an explanatory diagram showing an input image signal supplied to the control circuit and input signals supplied to first and second display sections, respectively, in another arrangement that is different from

the arrangement shown in Fig. 3.

DESCRIPTION OF THE EMBODIMENTS

The following description deals with one embodiment of the present invention by taking a liquid crystal display apparatus for example with reference to drawings. Note that the display apparatus of the present invention is applicable to a data holding display apparatus, and therefore the present invention is not necessarily limited to the liquid crystal display apparatus.

Fig. 1 is a view schematically showing a structure of an active matrix liquid crystal display apparatus (hereinafter referred to as liquid crystal display apparatus) in accordance with one embodiment of the present invention. As shown in Fig. 1, the liquid crystal display apparatus includes a display section 11 (display means), a scanning signal line driving circuit 12 (scanning signal line driving means), a data signal line driving circuit 13 (data signal line driving means), and a control circuit 14 (control means).

It is assumed that the display section 11 includes 480 scanning signal lines and 640 data signal lines, for example, according to the present embodiment. The display section 11 is divided into upper and lower display sections, i.e., first and second display sections 11a and 11b, respectively. The scanning signal lines are

perpendicularly provided, respectively. The first display section 11a includes 240 scanning signal lines, and the second display sections 11b also includes 240 scanning signal lines.

The scanning signal line driving circuit 12 is composed of first and second scanning signal line driving circuits 12a and 12b. The first scanning signal line driving circuit 12a (scanning signal line driving means) sequentially scans the scanning signal lines of the first display section 11a. The second scanning signal line driving circuit 12b (scanning signal line driving means) sequentially scans the scanning signal lines of the second display section 11b.

Note that the scanning signal line driving circuit 12 may be constituted by a single scanning signal line driving circuit. For convenience, this embodiment deals with the case where the scanning signal line driving circuit 12 is composed of the first and second scanning signal line driving circuits 12a and 12b, respectively. This is for the purpose of making clear how the first and second the display sections 11a and 11b relate to the scanning signal line driving circuit 12.

The data signal line driving circuit 13 includes first and second signal line driving circuits 13a and 13b, respectively. The first signal line driving circuit 13a (first data signal line driving means) supplies the data signal

lines of the first display section 11a with the display data. The second signal line driving circuit 13b (second data signal line driving means) supplies the data signal lines of the second display section 11b with the display data.

The control circuit 14 generates signals/data such as (a) control signals for instructing the timings at which the first and second scanning signal line driving circuits 12a and 12b should operate, respectively, and (b) display data and display data for use in the interpolation which are essence of the generation of the display signals to supply the first and second signal line driving circuits 13a and 13b. The control circuit 14 also generates other signals/data and supplies them to their associated circuits.

The first display section 11a of the display section 11 includes 240 scanning signal lines Y1 through Y240 and 640 data signal lines X1 through X640 constituting a first data signal line group (see Fig. 2). A pixel is provided at each intersection of the scanning signal lines and the data signal lines. The second display section 11b of the display section 11 includes 240 scanning signal lines Y241 through Y480 and 640 data signal lines XX1 through XX640 constituting a second data signal line group. A pixel is provided at each intersection of the scanning signal lines and the data signal lines.

The writing of the display signal into each pixel is

carried out by selecting the scanning signal line such that the TFT, connected to the scanning signal line, turns on and then the display signal of the data signal line, connected to the TFT that has turned on, charges the liquid crystal capacity of the pixel.

Here, the first data signal line group is for writing of the display signal into the first display section 11a, whereas the second data signal line group is for writing of the display signal into the second display section 11b. The first and second data signal line groups include 640 data signal lines, respectively.

Fig. 3 is an explanatory view showing image signal (photographic image) and showing display signals corresponding to the image signals that are supplied to the first and second display sections 11a and 11b, respectively. In Fig. 3, one display period of the input image signal corresponds to one frame.

In Fig. 3, symbol "A" indicates image signal or display data (display signal) corresponding to the first display section 11a, and symbol "B" indicates image signal or display data (display signal) corresponding to the second display section 11b. The reference numerals written in addition to symbols "A" and "B" indicate frame numbers, respectively. Lower-numbered reference numeral indicates earlier frame. Symbol "A0·A1" that is inputted into the first display section 11a in the first half of one

frame or symbol "B0·B1" that is inputted into the second display section 11b in the second half of the one frame, etc., indicate interpolation display data (interpolation display signal), respectively.

During one frame period, the control circuit 14 receives, as usual in chronological order, the image signal corresponding to the display signal that is supplied to the first display section 11a and the image signal corresponding to the display signal that is supplied to the second display section 11b.

In contrast, the display signals are simultaneously (collaterally) supplied to the first and second display sections 11a and 11b. Note that it is preferable that the display signals are simultaneously supplied to the first and second display sections 11a and 11b because of the reasons such as the easiness of control, but the present invention is not limited to this, provided that the display signals are overlapped in terms of time.

When adopting a conventional technique, the writing of the display signal into the pixel of the display section 11 is carried out once in one frame period. In contrast, according to the present liquid crystal display apparatus, the writings of the display signals into the first and second display sections 11a and 11b are carried out collaterally in terms of time. This ensures that the display signal is written into the pixel twice during one frame

period without changing the writing speed, i.e., without increasing the writing speed. Thus, it is possible in the present liquid crystal display apparatus that the original display signal and other interpolation display signal are written into the pixel during one frame period.

In the example shown in Fig. 3, the interpolation display data "A0 · A1" is assigned to the first display section 11a in the first half of one frame period and the display data "A1" is assigned to the first display section 11a in the second half of the one frame period. In contrast, the display data "B0" is assigned to the second display section 11b in the first half of one frame period and the interpolation display data "B0 · B1" is assigned to the second display section 11b in the second half of the one frame period.

The interpolation display data "A0 · A1" is obtained by using (a) the first half section of one frame period of an input image signal that is one frame earlier than a current input image signal and (b) the first half section of one frame period of the current input image signal. The display data "A1" is obtained by using only the first half section of one frame period of the current input image signal.

The display data "B0" is obtained by using only the second half section of one frame period of the input image signal that is one frame earlier than the current input

image. The interpolation display data "B0·B1" is obtained by using (a) the second half section of one frame period of the input image signal that is one frame earlier than the current input image signal and (b) the second half section of one frame period of the current input image signal.

The similar relation between the display data of the first display section 11a and the display data of the second display section 11b is found in other frame periods.

In the present embodiment, the simultaneous writings into the pixels start while the first and second display sections 11a and 11b are scanned in descending order. Thus, in a single frame, the time difference between the time when the writing into the lowermost scanning signal line Y240 of the first display section 11a starts and the time when the writing into the uppermost scanning signal line Y241 of the second display section 11b is equal to about 0.5 frame. On this account, it looks like the continuity of the first and second display sections 11a and 11b is not entirely maintained.

However, according to the display shown in Fig. 3, for example, the continuity of (a) the display data A1 of the first display section 11a of the second half of the current frame and (b) the display data B1 of the second display section 11b of the first half of the next frame is maintained (see Fig. 4). The continuity of (a) the

interpolation display data "A0 · A1" of the first display section 11a of the first half of the current frame and (b) the interpolation display data "B0 · B1" of the second display section 11b of the second half of the current frame is almost maintained.

Accordingly, the combination shown in Fig. 3 is preferable for the generation of the display data to reduce the time deviation between (a) the display signal to be supplied to the pixel corresponding to the scanning signal line Y240 (the first display section 11a) and (b) the display signal to be supplied to the pixel corresponding to the scanning signal line Y241 (the second display section 11b). Note that the generation of the display data shown in Fig. 3 is not necessarily required if it is not limited to the case where the scanning signal lines are scanned in descending order.

Fig. 5 is a block diagram showing an arrangement of a display data generating section 21 in the control circuit 14. The display data generating section 21 generates the display data to supply to the first and second signal line driving circuits 13a and 13b. The display data generating section 21 includes a memory 22, an arithmetic circuit 23 (arithmetic means), and a selector 24. The memory 22 is not limited to a specific one, provided that it has enough memory capacity to store the input image signal corresponding to the first display section 11a or second

display section 11b. Note that circuits such as flip-flops for correcting the deviations of the respective circuits are omitted from the arrangement shown in Fig. 3, for convenience. Note also that the following description deals with the arrangement of the display data generating section 21 for the first display section 11a.

First, the input image signal corresponding to the first display section 11a is stored in the memory 22, and is supplied to the arithmetic circuit 23. Vertical synchronization is used as the basis for the operation timings of the memory 22 and the selector 24. Upon being read out from the memory 22, the input image signal that has been stored in the memory 22 is supplied as the display signal to the arithmetic circuit 23 and the selector 24, respectively.

The arithmetic circuit 23 prepares the interpolation display data in accordance with the input image signal and the display data that has been read out from the memory 22, and supplies the selector 24 with the interpolation display data thus prepared. The selector 24 selects either one of the display signal and the interpolation display data in accordance with the timing of a display switching signal which is generated on the basis of the vertical synchronization timing, and supplies the selected signal to the following first signal line driving circuit 13a as an output signal.

Note that an arrangement of the display data generating section 21 for the second display section 11b is basically similar to that for the first display section 11a, except that the timing, for selecting either one of the display data to be supplied to the second signal line driving circuit 13b and the interpolation display data, comes 0.5 frame period later after the timing for the first display section 11a.

The following description deals with the interpolation display data.

It is preferable that the level (gradation level) of the interpolation display data is an intermediate level between the levels of the respective input image signals of the two target frames to be interpolated. This is because of the purpose of interpolating an inter-frame signal in the display section 11.

When taking the simplification of the arithmetic circuit 23 into consideration, it is preferable that the interpolation display data is an average of the levels of the respective input image signals of the two target frames to be interpolated. This is because the average can be obtained for digital input image signals, merely, by adding the levels of the input image signals of the two frames and by carrying out a bit shift after the addition, thereby ensuring the simplification of the arithmetic circuit 23.

Fig. 6 is an explanatory diagram showing a range

within which the interpolation display data "A0·A1" may fall. In Fig. 6, the range within which the interpolation display data "A0 · A1" may fall is denoted as the arrowheads. Namely, it is possible to set the level of the interpolation display data "A0·A1" so as to be greater than the display data A0 and so as to be smaller than the display data A1.

Ideally, as mentioned above, the level of the interpolation display data is an intermediate level between the levels of the display data A0 and A1. Fig. 7 shows a concrete arrangement of the arithmetic circuit 23 in the case of finding the interpolation display data having the above level.

According to the arrangement shown in Fig. 7, the levels of the respective display data A0 and A1 are added by an adder 31, and then an output signal of the adder 31 is divided by a divider 32, so that one half of the addition of the display data A0 and A1 is obtained. The concrete operation of the divider 32 is to carry out 1-bit shift with respect to the added result of the adder 31.

The present invention is not limited to the case where the level of the interpolation display data is merely the average of the display data A0 and A1. The level of the interpolation display data may be the weighted interpolation display data. The way to weight the interpolation display data may be selectable at the

discretion of the circuit designer. For example, the interpolation display data may be weighted in accordance with the direction along which the display data changes. More specifically, in the case of changing from display data A0 of a previous frame to display data A1 of a current frame, the interpolation display data may be weighted in the direction toward the level of the display data A1. The concrete arrangement of the arithmetic circuit 23 for obtaining the interpolation display data thus weighted is shown in Fig. 8.

According to the arrangement shown in Fig. 8, an adder 31 carries out addition once with respect to the level of the display data A0, whereas three adders 31 carry out addition totally thrice with respect to the level of the display data A1. A divider 33 divides a finally added result, so that one fourth of the added result is obtained. The concrete operation of the divider 33 is to carry out 2-bit shift with respect to the finally added result. D-type flip-flops 34 are provided merely for obtaining of timings.

The arrangement of the arithmetic circuit 23 for determining the interpolation display data is not limited to the above arrangement. Other arrangements may be adopted. For example, as shown in Fig. 9, the arrangement in which a look-up table is provided for outputting the interpolation display data "A0 · A1" in response to the display data A0 and A1 is used.

As has been described above, in the liquid crystal display apparatus of the present invention, the display section 11 is divided into the first and second display sections 11a and 11b, respectively, and the first and second display sections 11a and 11b are driven independently and collaterally. In this case, the display signal corresponding to the input image signal is supplied to one of the first and second display sections 11a and 11b, for example, the first display section 11a (each pixel of the first display section 11a) in the first half of one frame period, while the interpolation display signal (interpolation display data) prepared in accordance with the input image signal is supplied to the other of the first and second display sections 11a and 11b, for example, the second display section 11b (each pixel of the second display section 11b). For example, the interpolation display signal is prepared in accordance with a current input image signal and an input image signal that is one frame earlier than the current input image signal. In the second half of the one frame period, the display signals (display data) are respectively supplied to the first and second display sections 11a and 11b in a reverse manner. More specifically, in the second half of one frame period, the interpolation display signal that is prepared in accordance with the input image signal is supplied to the first display section 11a (each pixel of the first display

section 11a), while the display signal corresponding to the input image signal is supplied to the second display section 11b (each pixel of the second display section 11b).

According to the present liquid crystal display apparatus, the display signal is written at a double speed into the entire display section 11 during one frame period. Namely, the frame frequency becomes twice. This ensures to restrain the blurring of the moving image during the displaying.

Further, according to the present liquid crystal display apparatus, the display signal corresponding to the input image signal is written into one of the display sections, whereas the interpolation display signal that is prepared in accordance with the input image signal is written into the other of the display sections. This ensures to avoid that the brightness of the entire display screen is lowered, unlike the case where the black display signal is merely written.

In addition, although the display signal is written into the display section 11 in its entirety at a double speed, it is not necessary to write the display signal into each of the first and second display sections 11a and 11b at such a double speed. Accordingly, it is possible to fully secure a response time of the liquid crystal required for writing the display signal.

As mentioned above, it is preferable that the

interpolation display signal is prepared in accordance with a current input image signal and an input image signal that is one frame earlier than the current input image signal. The present invention is however not limited to this, provided that the interpolation display data is prepared in accordance with the input image signal.

The foregoing description deals with the case where the display section 11 is divided into two. The present invention is not limited to this. The display section 11 may be divided into three or more sections. In this case, it is necessary to provide signal line driving circuits whose number is equal to the number of the divisions of the display section 11, and it is necessary that the control circuit 14 supplies each of the respective signal line driving circuits with (a) display data corresponding to the input image signal and (b) an interpolation display signal prepared in accordance with the input image signal.

The foregoing description deals with the case where the display signal is written into the display section 11 twice during one frame period. Thrice or more, the display signal may be written into the display section 11 during one frame period. Alternatively, the number of the writing of the display signal into the display section 11 may be determined in accordance with the number of the divisions of the display section 11.

Fig. 10 shows the case where (a) the display section

11 is divided into three sections, for example, in such a direction that the scanning signal lines are provided and (b) the number of the writing of the display signal into the display section 11 during one frame period is three, this number being coincident with the number of the divisions of the display section 11.

In Fig. 10, the display section 11 is divided into first through third display sections 11p through 11r. Each of the first through third display sections 11p through 11r includes the same number of the scanning signal lines, for example. Like the case shown in Fig. 1, first through third signal line driving circuits are provided so as to correspond to the first through third display sections 11p through 11r, respectively. One frame period is divided into first through third time periods, each of which has one third of one frame period, for example. In each of the first through third time periods, the control circuit 14 supplies the first through third signal line driving circuits with display data corresponding to an input image signal or with interpolation display data prepared in accordance with the input image signal. This ensures that (a) the display data corresponding to an input image signal or (b) the interpolation display data prepared in accordance with the input image signal is thrice written into each display section during one frame period.

For example, the writing of the display signal into

the display section 11 is carried out trice: the input image signal itself (the display signal corresponding to the input image signal) is once written into the display section 11; and the interpolation display signal prepared in accordance with the input image signal is twice written into the display section 11. In this case, it is preferable that the interpolation display signal to be twice written into the display section 11 is generated so as to interpolate between the input image signals, thereby resulting in that the continuity of the image (video picture) is maintained on the display section 11.

More specifically, as shown in Fig. 10, interpolation display data "A1 · A2" is assigned for the first display section 11p during the first and second time periods in one frame period, whereas interpolation display data "A2" is assigned for the first display section 11p during the third time period in one frame period. Interpolation display data "B1" is assigned for the second display section 11q during the first time period in one frame period, whereas interpolation display data "B1 · B2" is assigned for the second display section 11q during the second and third time periods in the one frame period. Interpolation display data "C0 · C1" is assigned for the third display section 11r during the first time period in one frame period, interpolation display data "C1" is assigned for the second display section 11r during the

second time period in the one frame period, and interpolation display data "C1 · C2" is assigned for the third display section 11r during the third time period in the one frame period.

Note that the display data A, B, and C correspond to the first, second, and third display sections 11p, 11q, and 11r, respectively.

In Fig. 10, the continuity of (a) the interpolation display data "A1 · A2" in the first display section 11p during the first time period of the current frame, (b) the interpolation display data "B1·B2" in the second display section 11q during the second time period of the current frame, and (c) the interpolation display data "C1·C2" in the third display section 11r during the third time period of the current frame is maintained. The continuity of (a) the interpolation display data "A1·A2" in the first display section 11p during the second time period of the current frame, (b) the interpolation display data "B1·B2" in the second display section 11q during the third time period of the current frame, and (c) the interpolation display data "C1·C2" in the third display section 11r during the first time period of the next frame is maintained. The continuity of (a) the interpolation display data "A2" in the first display section 11p during the third time period of the current frame, (b) the interpolation display data "B2" in the second display section 11q during the first time

period of the next frame, and (c) the interpolation display data "C2" in the third display section 11r during the second time period of the next frame is maintained.

The above description deals with the case where the present invention is applied to an active matrix liquid crystal display apparatus. However, the present invention is not limited to this. The present invention may be applied to any data holding active matrix display apparatus.

The present invention is not limited to the respective embodiments. The present invention may be modified in many ways within a range recited in claims. The technical scope of the present invention also includes an embodiment obtained by appropriately combining the technical means disclosed in the above-described different embodiments.

As has been described above, a data holding display apparatus in accordance with the present invention includes: (a) display means of data holding type for displaying a display signal, the display means including: a plurality of scanning signal lines; a plurality of data signal lines provided so as to intersect with the scanning signal lines; and pixels provided in a matrix manner at respective intersections of the scanning signal lines and the data signal lines; the display means having a display area which is divided, in a direction where the scanning

signal lines are provided, into a plurality of display sections each capable of being independently driven, and in said display means the display signal being written into data signal lines connected to pixels of the display section that have been selected, (b) scanning signal line driving means for sequentially selecting the scanning signal lines, (c) data signal line driving means, provided for the respective display sections, for supplying the data signal lines with the display signal corresponding to inputted display data, and (d) control means for (1) controlling the scanning signal line driving means such that the scanning signal lines in the respective display sections are scanned collaterally and the scanning signal lines in the respective display sections are sequentially selected during a plurality of time periods of one cycle in a displaying of the display means, so as to repeatedly scan the respective display sections in the one cycle as many times as the number of the time periods, and (2) supplying the data signal line driving means of the respective display sections with either one of the display data corresponding to an input image signal and an interpolation display data prepared in accordance with the input image signal during at least one of the time periods whereas with the other during at least one other time period.

With the arrangement, it is possible to separately drive the display sections, which are obtained by dividing

the display area of the display means, collaterally by the respective data signal line driving circuits that correspond to the display sections. The scanning signal lines of the respective display sections are sequentially selected during the plural time periods (for example, the number of the time periods is equal to the number of display sections) in one cycle (for example, one frame). This ensures that the respective display sections are repeatedly scanned in the one cycle as many times as the number of the plural time periods. For example, the input image signal is decomposed to so as to correspond to the respective display sections, and the data signal line driving circuits of the respective display sections are supplied with either one of the display data corresponding to an input image signal and an interpolation display data prepared in accordance with the input image signal during at least one of the time periods, whereas supplied with the other during at least one other time period.

Accordingly, it is not necessary in the present data holding display apparatus to scan the scanning signal lines of the respective display sections at a high speed. Because of this, it is possible to secure enough time for writing the display data into the pixel and to secure enough response time of the display panel to the writing.

On the other hand, from the viewpoint of the entire display panel, the double speed driving, i.e., the

pseudo-double speed driving is carried out. This makes it possible to restrain that the display quality of moving image is deteriorated due to the fact that a same display data has been held by a same pixel for a long period of time.

Further, the interpolation display data is prepared in accordance with the input image signal. Accordingly, it is possible to avoid that the brightness on a display screen is lowered, which occurs when the interpolation display data is merely set to a black display data.

In the data holding display apparatus, it may be arranged such that the interpolation display data is prepared in accordance with (a) a current image signal of a current one cycle corresponding to the display section carrying out a display in accordance with the interpolation display data and (b) a neighboring image signal that is one cycle earlier or one cycle later than the current image signal.

With the arrangement, the interpolation display data is prepared in accordance with (a) a current image signal of a current one cycle corresponding to the display section carrying out a display in accordance with the interpolation display data and (b) a neighboring image signal that is one cycle earlier or one cycle later than the current image signal. This ensures that the continuity of a display image corresponding to the input image signal and an

interpolation image based on the interpolation display data is substantially maintained. It is possible to reduce residual image while facilitating the displaying, thereby improving the display quality of moving image.

In the data holding display apparatus, it may be arranged such that the interpolation display data has a signal level of (a) greater than a smaller one of the current image signal and the neighboring image signal and of (b) smaller than a greater one of the current image signal and the neighboring image signal, when these image signals are different from each other.

With the arrangement, it is possible to appropriately maintain the continuity of the display image corresponding to the input image signal and the interpolation image corresponding to the interpolation display data. This ensures to improve the facilitation of displaying the moving image.

In the data holding display apparatus, it may be arranged such that the interpolation display data has a signal level of an average of the current image signal and the neighboring image signal.

In the data holding display apparatus, it may be arranged such that the control means includes arithmetic means for calculating and finding the interpolation display data.

With the arrangement, the interpolation display data

is found by arithmetic operation based on the display data of one frame in the input image signal and the display data of another frame adjacent to the one frame, for example. On this account, it is possible to restrain and reduce the size of circuits constituting the control means.

In the data holding display apparatus, it may be arranged such that the one cycle in the displaying of the display means is one frame cycle of the input image signal.

With the arrangement, the cycle at which one image of the data holding display apparatus is displayed is one frame cycle. Thus, it is not necessary to provide a memory for synchronizing the input image signal with the interpolation image signal to be displayed in response to the interpolation display data, thereby simplifying the circuits for generating the interpolation image signal.

In the data holding display apparatus, it may be arranged such that a time deviation between the first and second time periods is equal to one half of a frame cycle.

In the driving method of the data holding display apparatus, it may be arranged such that a time deviation between the first and second time periods is equal to one half of a frame cycle.

With the arrangement, in the display area of the display means, the display signal varying depending on the display data corresponding to the input image signal

and the display signal varying depending on the interpolation display data have a same mix. This ensures to reduce the residual image, thereby enabling of displaying further excellent moving image.

In the data holding display apparatus, it may be arranged such that a time period required for the scanning signal line driving means to scan the first display section and a time period required for the scanning signal line driving means to scan the second display section are respectively one half of a frame period, and such that the first and second display sections are simultaneously scanned.

In the driving method of the data holding display apparatus, it may be arranged such that a time period required for the scanning signal line driving means to scan the first display section and a time period required for the scanning signal line driving means to scan the second display section are respectively one half of a frame period, and such that the first and second display sections are simultaneously scanned.

With the arrangement, it ensures that the continuity of (a) an image displayed, on the first display section, corresponding to the input image signal and (b) an image, on the second display section, corresponding to the input image signal is maintained. Further, the above two images are written continuously in terms of time into the first

and second display sections so as to bridge between the first and second display sections. Thus, it is possible to facilitate the displaying of the images corresponding to the input image signals, with bridging between the first and second display sections.

In the data holding display apparatus, it may be arranged such that one of the interpolation display data supplied to the data signal line driving means of the respective first and second display sections during one frame period is prepared in accordance with a first input image signal which is supplied to the data signal line driving means during one frame period and a second input image signal which is one frame earlier than the first input image signal, and such that the other of the interpolation display data is prepared in accordance with the first input image signal and a third input image signal which is one frame later than the first input image signal.

With the arrangement, in addition to the continuity of the image corresponding to the input image signals, it also ensures that the continuity of (a) an image displayed, on the first display section, corresponding to the interpolation display data and (b) an image, on the second display section, corresponding to the interpolation display data is maintained. Further, the above two images are written continuously in terms of time into the first and second display sections so as to bridge between the first

and second display sections. Thus, in addition to the facilitation of the displaying of the images corresponding to the input image signals, it is also possible to facilitate the displaying of the images corresponding to the interpolation display data input image signals, with bridging between the first and second display sections.

As described above, according to the data holding display apparatus in accordance with the present invention, it is possible in the display panel (mainly, liquid crystal display panel) to restrain the lowering of brightness and the deterioration of the display quality of moving image. It is possible to suitably use the present data holding display apparatus in a television set including a liquid crystal display panel.

Further, it is possible to suitably use the present data holding display apparatus in a hand-held device such as PDA (Personal Digital Assistants) or a cellar mobile telephone which includes a liquid crystal display panel and can carry out the displaying of moving image.

The present data holding display apparatus is applicable to any apparatus that can carry out the displaying of moving image.

The invention being thus described, it will be obvious that the same way may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such

modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.